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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,625	05/24/2006	Raymond J. E. Hueting	GB03 0212 US	4378

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EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
06/09/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/580,625	HUETING ET AL.	
	Examiner	Art Unit	
	HSIN-YI HSIEH	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 01/19/2011, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Lynne A. Gurley/

Supervisory Patent Examiner, Art Unit 2811.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1, 4-7, 9-10, 12-19 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (EP 1168455 A2) in view of Peake et al. (US 2005/0173758).

5. Omura et al. teach, regarding to **claim 1**, an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the

first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and a doping concentration in the drift region (12) increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11; see Fig. 15B, paragraph [0053]), regarding to **claim 15**, an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type;

paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode(19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and wherein the drift region (12) has a graded doping concentration (see Fig. 15B) that increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11; see Fig. 15B), and regarding to **claim 19**, an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the

top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) at the first major surface (the top surface of 13), a body region (well layer 13; Fig. 2, paragraph [0023]) under the source region (14), a drift region (drift layer 12; Fig. 2, paragraph [0023]) under the body region (13), and a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) under the drift region (12), the drift region (12) having a doping concentration (see Fig. 15B) that increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11); and a plurality of insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) into the drift region (12), each of the insulated trenches (15) including at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) and separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) and separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]).

Omura et al. do not teach, regarding to **claim 1**, the gate-field plate insulator (18) being at least as thick as the field plate insulator (16), and the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13), regarding to **claim 15**, the gate-field plate insulator (18) being thicker than the field plate insulator (16), the doping concentration in the part of the drift region (12) adjacent to the drain

region (11) being at least 50 times greater than the doping concentration in the part of the drift region (12) adjacent to the body region (13), and regarding to **claim 19**, the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13) and the gate-field plate insulator (18) being at least as thick as the field plate insulator (16).

In the same field of endeavor of trench-gate semiconductor device, Peake et al. teach, regarding to **claim 1**, the gate-field plate insulator (insulating material 26 of thickness t2 between the gate 8 and the field plate 24; Fig. 1, paragraph [0032]) being at least as thick as the field plate insulator (insulating material 26 of thickness t4 between the sidewalls of the field plate 24 and the semiconductor body, and t2 is preferably greater than t4; Fig. 1, paragraph [0032]), regarding to **claim 15**, the gate-field plate insulator (insulating material 26 of thickness t2 between the gate 8 and the field plate 24; Fig. 1, paragraph [0032]) being thicker than the field plate insulator (insulating material 26 of thickness t4 between the sidewalls of the field plate 24 and the semiconductor body, and t2 is preferably greater than t4; Fig. 1, paragraph [0032]), and regarding to **claim 19**, the gate-field plate insulator (insulating material 26 of thickness t2 between the gate 8 and the field plate 24; Fig. 1, paragraph [0032]) being at least as thick as the field plate insulator (insulating material 26 of thickness t4 between the sidewalls of the field plate 24 and the semiconductor body, and t2 is preferably greater than t4; Fig. 1, paragraph [0032]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Peake et al. and use the gate-field plate insulator being thicker than the field plate insulator as taught by Peake et al., because a relative

thick insulating layer is needed between the field plate and the gate to withstand the potential difference therebetween as a bias potential is applied to the field plate as taught by Peake et al. (paragraph [0032]).

Furthermore, parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

6. Regarding **claim 4**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.

Omura et al. teach a device with a breakdown voltage of 50V (paragraph [0045]). Omura et al. also teach that the breakdown voltage and the ON resistance satisfy the inequality: $Ron < 2.2 \times 10^{-5} Vb^{2.25}$.

Parameters such as the breakdown voltage and the ON resistance in the art of semiconductor manufacturing process are the tradeoff between the device's performance and reliability and are subject to changes due to the requirement of the application, e.g. whether the performance (lower ON resistance) is more important than the reliability (higher break down

voltage). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to lower the breakdown voltage to less than or equal to 30V as claimed in order to achieve a lower ON resistance to improve device performance.

7. Regarding **claim 5**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions (14) and the insulated trenches (15) arranged across the first major surface (the top surface of 13) is a pattern in which cells repeat in more than one direction across the first major surface (the top surface of 13) to form a three-dimensional cell structure (see Fig. 25).

8. Regarding **claim 6**, Omura et al. also teach an insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern (see Fig. 25)

9. Regarding **claim 7**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]) extending through the source region (14) to the body region (13) to connect a source contact (source electrode 21) to the source region (14) and the body region (13; see Fig. 4).

10. Regarding **claim 9**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein a thickness of the insulator (16; Fig. 2) adjacent to the conductive field plate electrode (17) is greater than a thickness of the insulator (18) adjacent to the conductive gate electrode (19; see Fig. 2, paragraph [0031]).

11. Regarding **claim 10**, Omura et al. teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells (Fig. 25).

Omura et al. do not teach the pattern of cells has a cell pitch not greater than 1 micron.

Parameters such as the cell pitch in the art of semiconductor manufacturing process are subject to change due to the requirement of the device performance. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use a cell pitch not greater than 1 micron as claimed to achieve the required performance.

12. Regarding **claim 12**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the field plate insulator (16) has a thickness between 0.6 to 1 microns and the gate insulator (18) has a thickness between 0.2 to 0.5 microns.

Omura et al. teach that the thickness of the field plate oxide (16) is determined by the breakdown voltage and the thickness of the gate oxide (18) is determined by the threshold voltage (paragraph [0031]) Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to have the thickness of the field plate oxide and the thickness of the gate oxide as claimed as a result of achieving a desired or required breakdown voltage and threshold voltage.

13. Regarding **claim 13**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode (17) is connected to the source region (21; Fig. 3, paragraph [0026])

14. Regarding **claim 14**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently (this is implied in the paragraph [0027], where Omura et al. disclose a voltage applied to each buried electrode 17, which obviously need a terminal connected to the buried electrode 17 to control the voltage).

15. Regarding **claims 16-17**, Omura et al. teach the doping concentration (Fig. 15B), the drift region (12), the drain region (11), the body region (13).

Omura et al. do not teach, regarding to **claim 16**, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 200 times greater than the doping concentration in the part of the drift region adjacent to the body region, regarding to **claim 17**, the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region,

Parameters such as the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003], or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the doping concentration within the range as claimed in order to achieve desired device performance.

16. Regarding **claim 18**, Omura et al. teach further comprising a source contact (source electrode 21; Fig. 4, paragraph [0026]) and an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]), the additional trench (the trench formed between the interlevel dielectric films 22) extending through the source region (14) to the body region (13), the conductive material in the additional trench (the

conductive material of the source electrode 21 in the trench) connecting the source contact (21) to the source region (14) and to the body region (13).

17. Regarding **claim 21**, Omura et al. teach an insulated gate field effect transistor according to claim 15, wherein the drift region (12) has a steeply graded doping concentration (see Fig. 15B).

Omura et al. do not teach the drift region has a steeply graded doping concentration that is defined by the ratio of the doping concentration of the part of the drift region adjacent to the drain region to the doping concentration of the part of the drift region adjacent to the body region and wherein the ratio is greater than at least one of: 50, 100 or 200.

Parameters such as the ratio of the doping concentration of the part of the drift region adjacent to the drain region to the doping concentration of the part of the drift region adjacent to the body region in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the ratio of the doping concentration of the part of the drift region adjacent to the drain region to the doping concentration of the part of the drift region adjacent to the body region within the range as claimed in order to achieve desired device performance.

18. **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. and Peake et al. as applied to claim 1 above, and further in view of Onda et al. ("SIC

Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol. 162, no. 1, 16 July 1997, pages 369-388).

Omura et al. teach, regarding to **claim 11**, the first conductivity type is n-type (the conductivity type of the source region; paragraph [0023]), the second conductivity type is p-type (the conductivity type of the body region; paragraph [0023]).

Omura et al. do not teach, regarding to **claim 2**, the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type (i.e. p-type), and regarding to **claim 11**, the conductive gate electrode is of p-type doped polysilicon.

In the same field of endeavor of semiconductor device, Onda et al. teach the conductive gate electrode is a p-type doped polysilicon (Fig. 1, page 371 line 27). Onda et al. also teach that p-type polysilicon is used to form an accumulation mode SiC trench MOSFET (page 371, lines 23-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al., Peake et al., and Onda et al. and use the gate taught by Onda et al., because an accumulation mode SiC trench MOSFET can be formed as taught by Onda et al.

19. **Claims 3 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. and Peake et al. as applied to claims 1and 19 above, and further in view of Miyano et al. (JP 403211885A).

Regarding **claims 3 and 20**, Omura et al. teach the conductive gate electrode and the insulated trench.

Omura et al. do not teach, regarding to **claim 3**, the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning a gap between the side pieces, and regarding to **claim 20**, the conductive gate electrode in each of the insulated trenches includes two vertical side pieces spaced apart from each other and adjacent to sidewalls on either side of the insulated trench, and a horizontal top piece spanning a gap between and connecting the two side pieces.

In the same field of endeavor of semiconductor device, Miyano et al. teach, regarding to **claim 3**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) has side pieces (the left side and the right pieces with deeper depth) spaced apart adjacent to the sidewalls on either side of the insulated trench (a trench; Fig. 1 and 2, [Application example]) and a top piece spanning a gap between the side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces), and regarding to **claim 20**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) in each of the insulated trenches (a trench; Fig. 1 and 2, [Application example]) includes two vertical side pieces (the left side and the right pieces with deeper depth) spaced apart from each other and adjacent to sidewalls on either side of the insulated trench (a trench; see Fig. 1 and 2, [Application example]), and a horizontal top piece spanning a gap between and connecting the two side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces).

Miyano et al. also teach the shape of the gate reduces the capacitance between the gate and the drain, i.e. the bottom structure, and a high speed operation can be performed ([Operation]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al., Peake et al., and Miyano et al. and use the gate taught by Miyano et al., because the speed of the device can be improved as taught by Miyano et al.

20. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. and Peake et al. as applied to claim 7 above, and further in view of Hshieh et al. (US 2001/0003367 A1).

Regarding **claim 8**, Omura et al. do not teach a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region.

In the same field of endeavor of vertical transistors, Hshieh et al. teach a doped contact region (P+ region 138; Fig. 2, paragraph [0025]) of the second conductivity type (p type) in the body region (in the P-body region; Fig. 2, paragraph [0025]) in contact with the conductive material (source metal layer 160; Fig. 2, paragraph [0025]) in the additional trench (source contact openings 150; Fig. 2, paragraph [0025]), a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region (the doping concentration of P+ region is higher than P region). Hshieh et al. also teach the doped contact region 138 is used to reduce the parasitic resistance (paragraph [0025]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al., Peake et al., and Hshieh et al. and use the doped

contact region taught by Hshieh et al., because the parasitic resistance can be reduced as taught by Hshieh et al.

Response to Arguments

21. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HSIN-YI HSIEH whose telephone number is (571)270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
6/1/2011